Microwave MESFET Mixer

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Abstract—**GaAs metal-semiconductor FET's (MESFET) are developed for use in amplifiers at microwave frequencies. The FET has a Schottky barrier between the gate and source, operating in the same manner as a Schottky-barrier diode. If the Schottky barrier is used as a mixer, the IF signal is generated and simultaneously amplified by the FET itself. Thus a mixer with IF preamplifier can be realized. In this paper the theoretical and experimental results of a FET mixer are described. In such operations, the conversion loss in the frequency conversion alone is large due to the high series resistance of the Schottky barrier. However, the overall FET mixer has a "conversion gain" because the IF gain of the FET is made large. The experimental conversion gain is 6 dB at the RF frequency of 10.8 GHz and the IF frequency of 1.7 GHz. The noise figure of the FET mixer is at present large (15 dB, for example), due to large conversion loss in the frequency conversion.**

I. Introduction

When field-effect transistors (FET's) are used as mixers [1], [2], the nonlinearity of FET's are utilized. A metal-semiconductor FET (MESFET) has two kinds of nonlinearities: One is the I_G–V_{GS} nonlinearity and the other is the I_D–V_{GS} nonlinearity. The former nonlinearity results from the Schottky barrier between gate and source and it shows characteristics analogous to Schottky-barrier diodes (SB diode) that are most useful for microwave mixers. The latter nonlinearity is caused by the pinch-off effect.

Since the FET mixers so far reported mainly utilized the I_D–V_{GS} nonlinearity, we have investigated the kind of mixer operating on the I_G–V_{GS} nonlinearity to demonstrate the possibilities of this type of mixer. The principle of this microwave mixer using a MESFET is as follows. The local-oscillator signal and input signal are applied between gate and source with zero bias voltage and are converted into the intermediate frequency (IF) across the SB gate. The converted signal controls the drain current and is amplified by the FET. This type of mixer is expected to have the following two features. 1) If the IF is chosen to be much lower than the cutoff of the FET to ensure large IF gain, the mixer will show an overall gain. At the same time, the SB gate still has a sufficient nonlinearity to convert the input signal, which has a frequency higher than the cutoff, down to an IF signal. 2) The transconductance (g_m) at a bias point (zero bias, for example) is constant, therefore the nonlinear distortion of the IF signal due to the I_D–V_{GS} nonlinearity seems to be as small as that of a SB diode mixer with FET preamplifier.

In this paper the performance of the FET as a microwave mixer is theoretically and experimentally discussed. First, the equivalent circuit, including the SB gate nonlinearity, is presented and the measurement of the circuit element values is discussed. Second, the frequency conversion process of the SB is analyzed using the conventional conversion theory, provided that the equivalent circuit constants are independent of the operation frequency. Finally, the experimental results are described. These results are compared with the calculated values.

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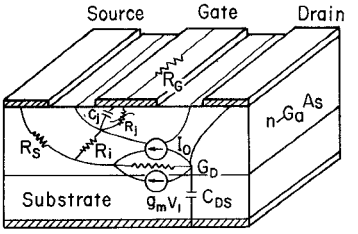

Fig. 1. Cross section of the MESFET with the equivalent circuit elements.

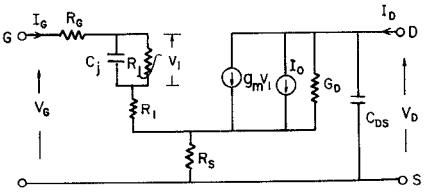

Fig. 2. The MESFET equivalent circuit and its parameters including the nonlinear resistor R_j of the SB and the drain bias current I_0.

II. An Equivalent Circuit and its Parameters

A cross-sectional view of a MESFET fabricated on semi-insulating substrate is shown in Fig. 1 [4], and it is also shown where the circuit elements are located. In Fig. 2 an equivalent circuit of a MESFET is shown in common source configuration.

Since a large local-oscillator voltage is applied to the gate when a MESFET is used as a frequency converter, a resistance R_j is added across C_j to take the nonlinearity of the SB conductance into consideration, which is essential for the mixing action. The dc bias current I_0 flowing from drain to source is included in the figure to take the variation of the bias voltage in the gate circuit, caused by I_0R_s drop, into consideration.

A. Gate Circuit when the Drain Circuit is not Biased

The current I_i through R_j can be expressed by the following equation:

$$I_i = I_s\left[\exp\left(\frac{eV_i}{\eta kT} - 1\right)\right] \simeq I_s \exp(\alpha_0 V_i) \qquad (1)$$

where

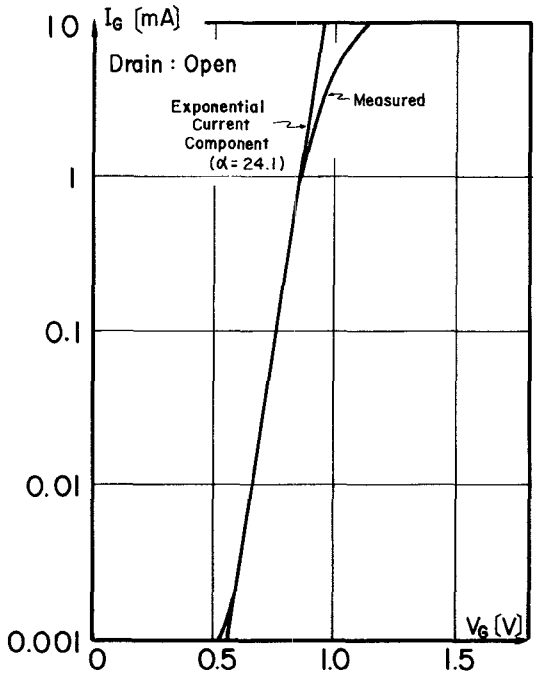

Fig. 3. I_G–V_G characteristic of the MESFET when the drain circuit is not biased.

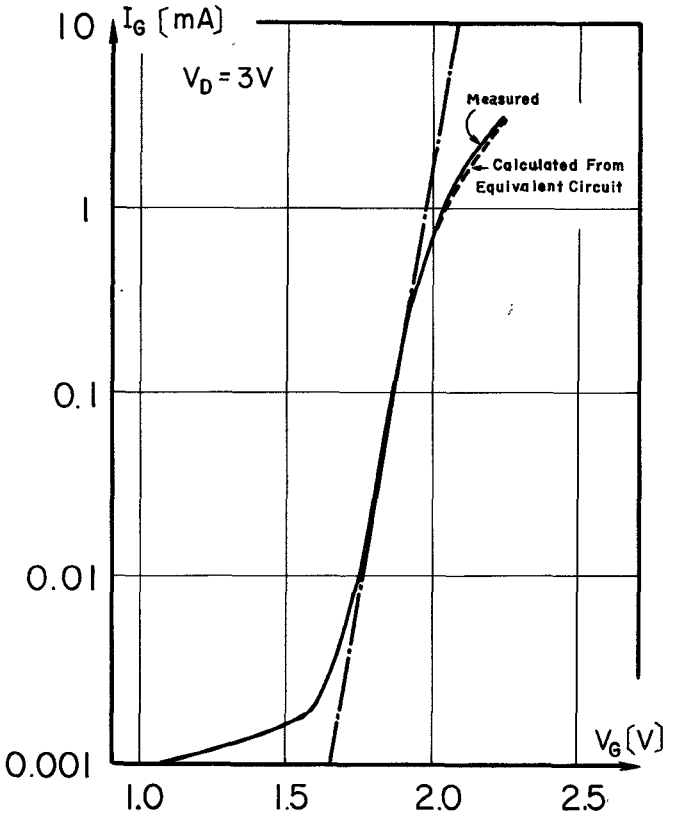

Fig. 4. I_G–V_G characteristic when drain circuit is biased.

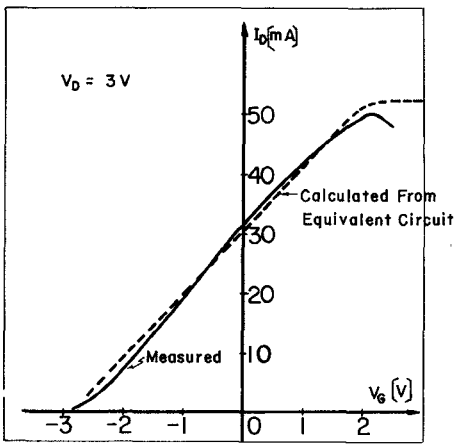

Fig. 5. I_D–V_G characteristic.

I_s saturation current;
k Boltzmann's constant;
T absolute temperature;
e electron charge;
V_i junction voltage;
η,α_0 constants.

For an open-circuited gate, the gate voltage is given as follows:

$$V_G = I_G R + (1/\alpha_0) \ln (I_G/I_s) \tag{2}$$

where

I_G gate current;
R total resistance of the gate circuit ($R = R_G + R_i + R_s$).

The experimental I_G–V_G characteristic is shown in Fig. 3.

When $I_G R \ll (1/\alpha_0) \ln (I_G/I_s)$ in (2) under small I_G conditions, V_G can be approximated by the second term in (2). Then α_0 and I_s can be obtained from the linear portion of the I_G–V_G characteristics shown in Fig. 3. R, the total resistance of the gate circuit, is then obtained from Fig. 3 and (2) with α_0 and I_s substituted. The measured values are

$$\alpha_0 = 24.1 \qquad I_s = 1.14 \text{ pA} \qquad R = 18.5\ \Omega.$$

B. Circuit Parameters when the Drain Circuit is Biased

When I_D is saturated with respect to V_D, then from Fig. 2, V_G and I_D can be expressed by the following equations:

$$V_G = V_i(I_G) + I_G R' + \{g_{m0} V_i(I_G) + I_0\} R_s' \tag{3}$$

$$I_D = I_0 + g_{m0} V_i(I_G) \tag{4}$$

where R' and R_s' represent R and R_s, respectively, when the drain circuit is biased. In (3) the first term means that the voltage developed across the junction is a function of I_G, which is supposed to be independent of the drain circuit conditions. The second term, the voltage drop of I_G across R', and the third term, the feedback voltage, is caused by I_D across R_s'. The parameters R_s', I_0, and g_{m0} can be obtained from the I_G–V_G and I_D–V_G characteristics shown in Figs. 4 and 5 by solid lines.

When I_G is so small that $I_G R'$ can be neglected, compared with the other two terms in (3), (5) is obtained

$$V_G = (1/g_{m0} + R_s') I_D - I_0/g_{m0}. \tag{5}$$

Equation (5) can be applied to Fig. 5 for $V_G < 1.85$ V, corresponding to $I_G < 100\ \mu$A in Fig. 4. In this case, the

solid line in Fig. 5 can be approximated by a straight line. This line is drawn, by the method of least squares, to make the values of $1/g_{m0} + R_s'$ and I_0/g_{m0} best fit the experimental results. They are

$$1/g_{m0} + R_s' = 92.8\ \Omega$$

and

$$I_0/g_{m0} = 2.80\ \text{V}.$$

From these results and the values of V_i, V_G, and I_D from Figs. 3–5 at sufficiently small I_G, values of R_s', I_0, and g_{m0} can be calculated from (3) and (4).

For example, if

$$I_G = 100\ \mu\text{A}$$

then

$$R_s' = 21.9\ \Omega$$

$$I_0 = 39.5\ \text{mA}$$

$$g_{m0} = 14.1\ \text{m}\mho.$$

With the previous parameter values substituted in (3) under the $I_GR' = 0$ condition, the I_G–V_G characteristic can be calculated and is shown by the dot–dash line in Fig. 4. The difference between the dot–dash line and the solid line in the region where $V_G > 1.85$ V shows the I_GR' drop. From this difference, R' is found to be 60 Ω. This value of 60 Ω and also $R_s' = 21.9\ \Omega$ are larger than the $R = 18.5\ \Omega$ obtained for zero drain bias. The reason for this change is not clear, but may be caused by the following. One reason is the deformation of the SB depletion layer due to electric fields between source and drain when drain bias is applied. The other reason is that the carrier mobility saturated and the incremental mobility reduced the region in the FET's active layer and effectively narrows the I_G channel compared to the case with zero drain voltage. Thus R' and R_s' become larger than R and R_s.

Using the values of the equivalent circuit constants obtained previously and using (3) and (4), the calculated I_G–V_G and I_D–V_G characteristics are shown by dotted lines in Figs. 4 and 5, respectively.

From the previous discussions, the following can be obtained.

1) The equivalent circuit shown in Fig. 2 can represent the behavior of the FET even when V_G is driven sufficiently positive. The saturation and reduction of I_D when V_G is very large, as shown in Fig. 5, is not caused by the nonlinearity of g_{m0}. This is explained in the following way.

a) Saturation of I_D: As V_G is increased positively, the ratio $R_j/(R_j + R')$ decreases due to the SB nonlinearity, which in turn reduces the V_i/V_G ratio. Thus the rate of change of $g_{m0}V_i$ with respect to V_G is also reduced, even at constant g_{m0}.

b) Reduction of I_D: Since the effective drain bias voltage is given by $V_D - I_DR_s'$, the reduction of I_D with respect to V_G is caused by a large I_DR_s' voltage drop with insufficient V_D at constant g_{m0}.

2) The slope of the linear portion of the I_G–V_G curve, shown in Fig. 4, is smaller than that of Fig. 3 by the factor $1/(1 + g_{m0}R_s')$, due to the negative feedback caused by the current $g_{m0}V_i$ flowing across R_s'. This change in the slope of the I_G–V_G curve can be considered as a change in α_0 under different drain circuit bias conditions. In the experiments, α_0 changes from 24.1 to 18.4.

C. G_D, C_{DS}, and C_j

1) G_D: G_D is experimentally obtained from the saturated region of the I_D–V_D characteristic as 0.5 m℧.

2) C_{DS}: C_{DS} can be tuned out by an external circuit and is neglected.

3) C_j: C_j is measured with a capacitance bridge at $V_{DS} = 3$ V, $V_{GS} = 0$ V, $f = 1$ MHz. The measured value is 0.4 pF.

We have assumed C_j to be constant for the following reasons. One is the complication in the theoretical calculation when the nonlinearity of C_j versus V_{GS} is considered; the other is the difficulty in measuring C_j when R_j is small.

III. Frequency Conversion in SB Junction

In this section the simple analysis of the frequency conversion is described. The assumption is made that the values of the equivalent circuit elements are frequency independent.

As mentioned in the last section, g_{m0} is nearly constant as long as the gate voltage is higher than the pinch-off voltage. Therefore, the transconductance under ac conditions g_m is considered to be linear with respect to the amplitude even if a large signal is applied. Hence, the frequency conversion is caused only by the SB junction. As far as frequency conversion in the SB junction is concerned, the conventional analysis of SB mixers is used [3].

The complex IF current I_{if} and the input signal current I_s are as follows:

$$\begin{bmatrix} I_{if} \\ I_s \end{bmatrix} = \begin{bmatrix} g_0 & g_1 \\ g_1 & g_0 \end{bmatrix} \begin{bmatrix} V_{if} \\ V_s \end{bmatrix} \tag{6}$$

where V_{if} and V_s are complex voltages at the IF and signal frequencies, respectively. g_0 and g_1 are given in the following equations:

$$g_0 = \alpha_0 I_s \exp(\alpha_0 V_0)\, \hat{I}_0(\alpha_0 V_l) \tag{7}$$

$$g_1 = \alpha_0 I_s \exp(\alpha_0 V_0)\, \hat{I}_1(\alpha_0 V_l) \tag{8}$$

where $\hat{I}_n$ is the modified Bessel function of the first kind of the nth order and V_0 and V_l are the dc bias and local oscillator voltages, respectively.

From Fig. 2 the gate voltages at the IF frequency, V_{Gif}, and at the input signal frequency, V_{Gs}, are as follows:

$$\begin{bmatrix} V_{Gif} \\ V_{Gs} \end{bmatrix} = \left[\left\{ \begin{pmatrix} g_0 & g_1 \\ g_1 & g_0 \end{pmatrix} + \begin{pmatrix} j\omega_{if}C_j & 0 \\ 0 & j\omega_s C_j \end{pmatrix} \right\}^{-1} + \begin{pmatrix} R' & 0 \\ 0 & R' \end{pmatrix} \right] \begin{pmatrix} I_{Gif} \\ I_{Gs} \end{pmatrix} = [z] \begin{bmatrix} I_{Gif} \\ I_{Gs} \end{bmatrix} \tag{9}$$

where I_{Gif} and I_{Gs} are gate currents at the intermediate and input signal frequencies, respectively. The capacitance between drain and gate C_{DG} is not considered in (9) for the following reasons.

Since C_{DG} is smaller than the junction capacitance C_j by an order of magnitude, C_{DG} can be neglected when com-

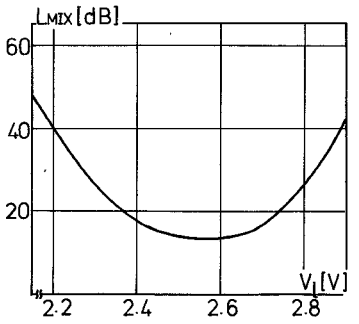

Fig. 6. Conversion loss in the MESFET's gate circuit.

pared to C_j at the signal frequency ω_s as the drain circuit is short circuited at ω_s. At the intermediate frequency, the effective capacitance across the gate terminal is $(g_{m0}/2G_D) \times C_{DG}$ due to the Miller effect. C_{DG} can also be neglected because the loading of the gate circuit due to the Miller effect has little influence on the junction voltage V_{if}. This will be shown later in Fig. 8.

From (9) it is shown that the input signal impedance that gives the minimum conversion loss is as follows [5]:

$$\begin{cases} Z_s = -\gamma_1 + \sqrt{\gamma_1^2 + \gamma_2}, & (10) \\ \gamma_1 = j\dfrac{\text{Im}\,(A^*D + BC^*)}{2\,\text{Re}\,(AC^*)}, \qquad \gamma_2 = \dfrac{\text{Re}\,(BD^*)}{\text{Re}\,(AC^*)} & (11) \end{cases}$$

where A, B, C, and D are the elements of the $ABCD$ matrix transformed from the $[Z]$ matrix. The asterisk denotes the complex conjugate. Re and Im denote the real and imaginary parts of the complex quantities, respectively. The IF impedance is

$$\begin{cases} Z_{if} = -\alpha_1 + \sqrt{\alpha_1^2 + \alpha_2}, & (12) \\ \alpha_1 = j\dfrac{\text{Im}\,(B^*C + A^*D)}{2\,\text{Re}\,(CD^*)}, \qquad \alpha_2 = \dfrac{\text{Re}\,(AB^*)}{\text{Re}\,(CD^*)} & (13) \end{cases}$$

and the minimum conversion loss is

$$L = \frac{\text{Re}\,(Z_s)}{\text{Re}\,(Z_{if})} \frac{|DZ_{if}^* + B|^2}{|Z_s|^2}. \quad (14)$$

The conversion loss versus local-oscillator voltage is shown in Fig. 6 using the parameters obtained in Section II. In Fig. 7 the impedance loci at the intermediate and input signal frequencies are shown versus local-oscillator voltage. At low voltage levels, the junction resistance R_j, which shows the nonlinear effect of the SB, becomes large and nearly linear so that the input signal impedance and the IF impedance are equal to $R' - j(1/\omega C_j)$, where ($\omega = \omega_s$ or ω_{if}) as shown in Fig. 7 by the points A and B, respectively. Thus the conversion loss is large.

On the other side, when the local-oscillator voltage is very large, both the input signal and the IF impedances move to the point C in Fig. 7. Since this point has an impedance of R', which means that the applied signal does not appear effectively across R_j, the conversion loss is also large. The minimum conversion loss is obtained at a suitable local-oscillator level, for example, 2.5–2.6 V in Fig. 6, and the minimum loss is about 14 dB. The minimum conversion loss is larger than in conventional SB diode mixers (about 5–6 dB in X band) because the total series resistance in this case is much larger than in a SB mixer diode.

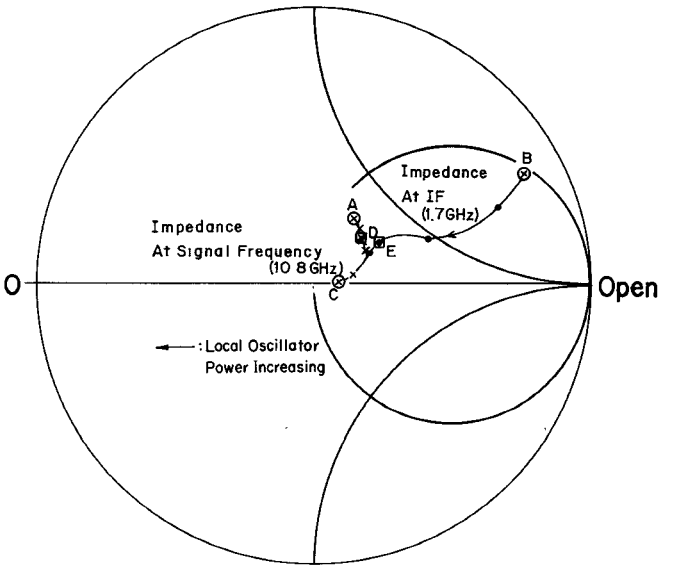

Fig. 7. Matched impedance of the gate circuit at intermediate and signal frequencies.

IV. Frequency Conversion and Amplification in a MESFET

In the previous section, only frequency conversion is discussed. In this section, frequency conversion and amplification, occurring simultaneously in a MESFET, are described.

From Fig. 2 the load impedance Z_{Dif}, which gives the maximum available power to the load in the drain circuit is

$$Z_{Dif} = \frac{1}{G_D} + R_s' \simeq \frac{1}{G_D}. \quad (15)$$

When the junction voltage at the IF is V_{if}, the maximum available power, P_{Dif}, is

$$P_{Dif} \simeq \frac{1}{4G_D} g_m^2 |V_{if}|^2. \quad (16)$$

$|V_{if}|$ depends on the gate impedance at the signal and intermediate frequencies. The conditions giving the maximum $|V_{if}|$ are now discussed.

From Fig. 2 and (9), the gate equivalent circuit can be obtained as shown in Fig. 8(a). In this figure, Z_{Lif} is the external circuit impedance. From Fig. 8(a), V_{if} normalized in respect to the input signal voltage can be obtained for the conditions that the input signal port is matched and Re (Z_{Lif}) is positive. V_{if} lies within the cross-hatched area shown in Fig. 8(b). The maximum $|V_{if}|$ is shown by the point located at the edge of the area corresponding to a reactive termination of the gate. This reactance, X_{mif}, is 201 Ω and is nearly equal to the reactance which resonates the IF circuit. The admittance appearing across the SB junction in the circuit is nearly constant due to the large conversion loss, even if the matching impedance of the signal circuit is changed. The maximum V_{if} is obtained

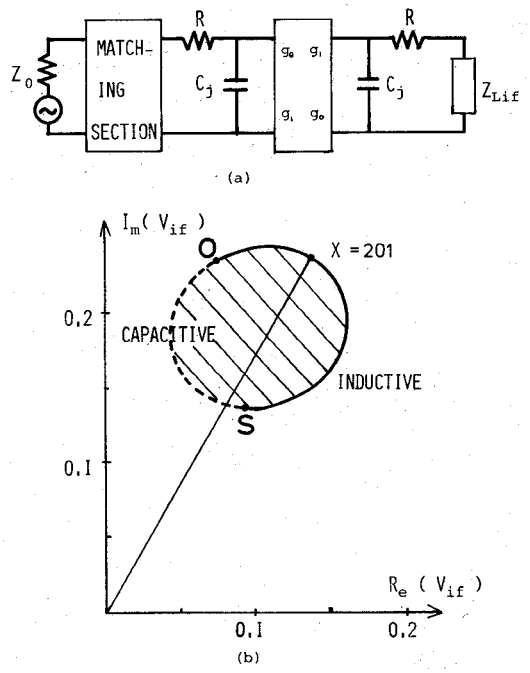

Fig. 8. The equivalent circuit of the MESFET gate as a mixer (a) and the junction voltage (b).

when the device gate impedance at the IF frequency is resonated by an external inductive reactance X_{mif}. The reactance X_{mif} is approximated by the following equation:

$$X_{mif} \simeq \frac{1 + \sqrt{1 - (2\omega_{if}C_jR)^2}}{2\omega_{if}C_j}. \tag{17}$$

Therefore, from (9) the input impedance at input signal frequency is

$$Z_{ms} = Z_{22} - \frac{Z_{12}Z_{21}}{jX_{mif} + Z_{11}}. \tag{18}$$

The maximum value of $|V_{if}|^2$ is

$$|V_{if}|^2 = P_{ins}\frac{1}{\mathrm{Re}\,(Z_{ms})}\left|Z_{12} + \frac{Z_{11}}{Z_{21}}(Z_{ms} - Z_{22})\right|^2 \cdot \left|\frac{R + jX_{mif}}{jX_{mif}}\right|^2 \tag{19}$$

where P_{ins} is the input power at the signal frequency. From (16) the overall conversion gain L_t is

$$L_t \simeq \frac{1}{4G_D}g_m^2|V_{if}|^2\frac{1}{P_{ins}}. \tag{20}$$

Using (20) and the parameters obtained, the "conversion gain" is calculated and shown by the solid line in Fig. 9. Comparing Fig. 9 with Fig. 6, it can be shown that the conversion gain is fairly large despite the large conversion loss in the gate circuit.

V. Experiment

In this experiment, the MESFET is mounted in a stripline circuit fabricated on a Teflon substrate as shown in Fig. 10. The local oscillator, signal, and intermediate frequency are chosen to be 9.1 GHz, 10.8 GHz, and 1.7 GHz, respectively.

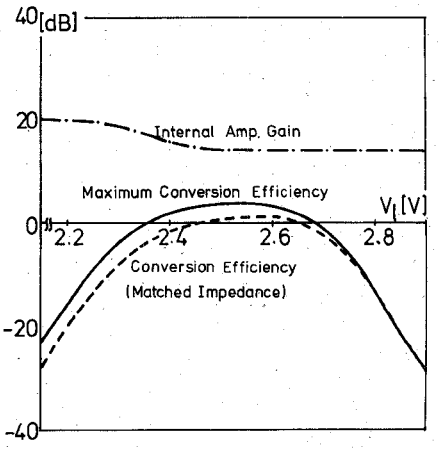

Fig. 9. Overall conversion gain of the MESFET mixer when the gate circuit is terminated by a matched impedance (dotted-line) and by reactance (solid-line).

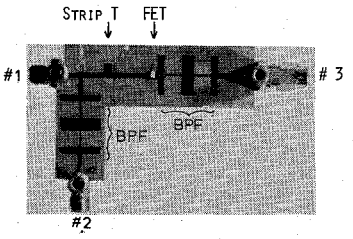

Fig. 10. Photograph of the experimental MESFET mixer.

To examine the effect of the external circuit on conversion gain at the IF, the IF signal is branched off by a filter and tuned by a stub tuner at port 2. In Fig. 10 the input signal is applied to port 1, the local oscillator to port 2, and the IF signal is extracted from port 3. The drain circuit is designed to present a short circuit at the signal and local-oscillator frequencies. The tuning of the gate circuit at the signal and intermediate frequencies is done in the following way.

First, the drain bias is set to the operating condition, and the gate bias set to yield an I_G in the range of 1–4 mA. This I_G is approximately equal to the rectified gate current under the operating conditions with local oscillator applied. Then port 1 is impedance matched at the signal frequency by a tuning stub and port 2 is matched at IF with a stub tuner.

Second, with all biases set at operating conditions and all signals applied, the fine tuning is adjusted to give minimum conversion loss at the gate circuit as monitored at port 2.

When port 2 is matched, the output power P_{Gif} from port 2 and P_{Dif} from port 3 are measured and shown in Fig. 11. In this experiment, the overall conversion gain is 1 dB, the conversion loss in the gate circuit is 17 dB. These results agree fairly well with the calculated values obtained from (14) for the gate circuit conversion loss and (21) for the overall conversion gain, both under impedance-matched conditions. Equation (21) is

$$L_t = (1/4G_D)g_m^2L\frac{|Z_{if} + R'|_2}{\mathrm{Re}\,(Z_{if})}. \tag{21}$$

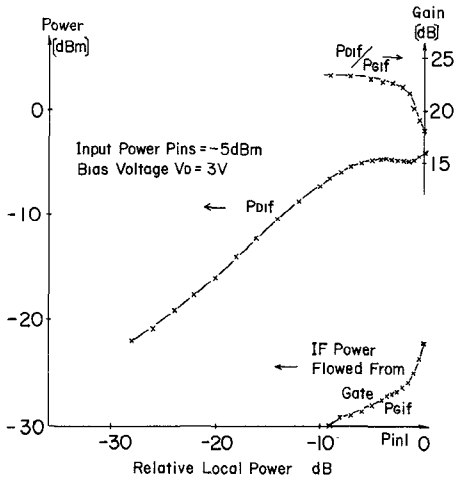

Fig. 11. Measured conversion gain of the MESFET mixer.

When port 2 is terminated by a reactance, and the drain output power P_{Dif} is maximized by adjusting the port 2 reactance, then the conversion gain increases up to 6 dB. This result agrees well with the calculated value.

The overall noise figure, with port 2 reactively terminated, is 15 dB. This large noise figure is considered to be caused by the large series resistance R' which makes the conversion loss large and by the high drain current, 30 mA in our experiment, as compared to that of a MESFET mixer using the pinch-off effect. One method to improve the noise figure is the reduction of the total gate circuit resistance R'.

VI. Conclusion

From the results of the theoretical and experimental investigations of FET mixers, it is shown that frequency conversion occurs in the SB between gate and source. The IF signal appears across the SB and is amplified by the FET. The equivalent series resistance in the FET's Schottky barrier is higher than in a conventional SB diode used in microwave mixers. This resistance increases with drain bias voltage due to the depletion layer deformation and the carrier mobility saturation. The conversion loss in X band (only considering mixing operation) is large (15 dB, for example). However, the overall mixer performance shows a "conversion gain" (6 dB, for example), because the IF (1.7-GHz) gain of the FET is larger than 20 dB. The experimental noise figure is as large as 15 dB, because the conversion loss is large due to the large series resistance in the SB and the large average drain current (30 mA, for example).

In applying an FET to a low-noise microwave receiver front-end for communication, FET's must be improved further. In particular, the FET must have a lower series resistance. The development of such FET's will enable us to design a monolithic receiver front-end and will replace present hybrid IC's.

Acknowledgment

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